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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/594,230

07/02/2007

Robert James Foulger

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EXAMINER

CHI, SUBERR L

ART UNIT

PAPER NUMBER

2829

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/594,230	Applicant(s) FOULGER ET AL.	
	Examiner SUBERR CHI	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/06/2011 has been entered.

Response to Arguments

2. The previously issued 112 2nd paragraph rejection(s) is withdrawn in view of canceled claim 9
3. The Applicant's arguments with respect to claims #1 and 2 in the reply filed on 06/06/2011 have been carefully considered, but are not persuasive and the previous rejection using Ho is retained for the reasons below.
4. As to the Applicants' arguments that Ho does not teach "selectively removing or breaking at least one electrically-conductive trace [40] by passing a current therethrough" because Ho teaches melting all the constricted segments at one time (**Applicants' Arguments submitted 06/06/11: page 11, lines 1-11**), the Examiner respectfully disagrees.

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The word “selectively” does not preclude the melting of all the constricted segments at one time, because the *particular selection is not specified*. Given that the claims recite “**at least one** support tab”, removal of one, two, or all support tabs could comprise selectively removing.

5. As to the Applicants’ arguments that Ho does not teach the functional limitation of “to controllably remove the respective discrete elements from the array”, the Examiner respectfully disagrees. The functional limitation does not distinguish the present invention over the prior art of Ho, who teaches the process as claimed. *Ho's process is capable of performing the functional limitation, however.*

Ho teaches that electrical current is passed through *each* of the electrically conductive constricting trace portions so as to leave open-circuit traces (**col. 2, lines 45-50**) by removing each trace from each plating bar (**Fig. 2B; col. 3, lines 64-67, col. 3, lines 1-2**). This is largely the same process as Ho’s prior art process (**col. 2, lines 10-15**), except that electric current is used instead of etchant. Ho’s prior art process also teaches that the result is to break each trace [40] away from each electrically conductive plating bar [20]. If each trace is removed from each plating bar, then it is possible to perform the functional limitation of removing Ho’s chips from the surrounding array portions. Ho’s open-circuit testing could not occur if all the traces were not broken from corresponding electrically conductive plating bars [20].

Claim Rejections 35 USC § 102(b)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim #1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ho.

6. As to claim 1, Ho teaches:

- a. *Manufacturing an array of said discrete elements (Fig. 1, [30]; col. 1, lines 23-32; individual package units obtained from singulating each package site) wherein each element is attached to at least one of an electrically conductive supporting structure (Fig. 1, [20]) and at least one other element (Fig. 1, neighboring chips [30] on adjacent package sites [11]) by at least one electrically conductive support tab (Fig. 1/2A, [40]).* The same structures are used for prior art Fig. 1 and exemplary embodiments of Figs. 2A/2B.
- b. *Selectively removing or breaking (Fig. 2B) the at least one support tab supporting one of the discrete elements, by passing a current therethrough to controllably remove the respective discrete elements from the array.* The constricted segment [41] portion of support tab [40] is broken by passing an electrical current; and each constricted segment is broken away from each corresponding electrically conductive

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plate bar [20] to form an open-circuit. Thus Ho's process is capable of performing the functional limitation of "*to controllably remove the respective discrete elements from the array*".

Claim Rejections - 35 USC § 103(a)

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103 that form the basis for the rejections under this section made in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim #2 is rejected under 35 USC 103(a) as being obvious over Ho in view of Ohkubo et al (US Patent #5,418,181, as cited in the IDS hereafter Ohkubo).

7. As to claim 2, Ho teaches:

- a. ***Manufacturing an array of devices (Fig. 1, [30]; col. 1, lines 23-32; individual package units obtained from singulating each package site) wherein each device is attached to at least one of an electrically conductive supporting mesh (Fig. 1, [20]) and at least one other device (Fig. 1, neighboring chips [30] on adjacent package sites [11]) by at least one electrically conductive support tab (Fig. 1/2A, [40]).*** The

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same structures are used for prior art Fig. 1 and exemplary embodiments of Figs. 2A/2B.

- b. *Selectively removing or breaking (Fig. 2B) the at least one support tab supporting one of the devices, by passing a current therethrough to controllably remove the devices from the array.* The constricted segment [41] portion of each support tab [40] is broken by passing an electrical current therethrough (**col. 3, lines 57-62**). Each constricted segment [41] portion of support tab [40] is broken by passing an electrical current; and each constricted segment is broken away from each corresponding electrically conductive plate bar [20] to form an open-circuit. Thus Ho's process is capable of performing the functional limitation of "*to controllably remove the respective discrete elements from the array*".

However, Ho does not teach the devices comprising Gunn diodes.

On the other hand, Ohkubo teaches devices comprising Gunn diodes (**Ohkubo: col. 1, lines 7-12**), for mass production.

It would have been obvious to one of ordinary skill in the art to combine the overall method of singulating individual devices using an electric current as taught by Ho, with devices such as Gunn diodes as taught by Ohkubo, because both Ho and Ohkubo are from the same field and endeavor and both are directed to producing discrete elements.

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Furthermore, the application of Ho's method towards the production of Gunn diode devices enables the predictable result of cost-effectively mass producing devices for high frequency applications, as Gunn diodes are suited towards.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUBERR CHI whose telephone number is (571)270-3955. The examiner can normally be reached on 9-5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571)272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SUBERR CHI/

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Examiner, Art Unit 2829

/HA TRAN T NGUYEN/

Supervisory Patent Examiner, Art Unit 2829